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Lab 7 Notes

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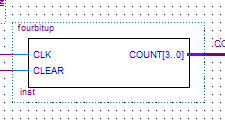
CSE 2441-001

**Introduction:** Lab 7 introduces the binary up/down counter along with a binary to seven segment display decoder. These decoders count up in hexadecimal on a single digit and also a two digit decimal displays located on the DE1.

**Theory:**  Building off a previous lecture a 4 bit binary up counter was produced in Verilog. This is also the first time a bus is utilized in contrition. A bus is helpful in carrying multiple signal lines to a location quickly and cleanly. Once a bus is built single wires maybe drawn from it by using an array syntax. For a bus that holds four lines like Lab 7 the syntax count[3..0], when a wire is to be split off from the bus it is indicated by this syntax count[0]. This will define wire 0 of the four wires in the bus ‘count’.

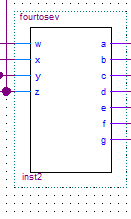
The first module that is created is the four bit up counter completely constructed in Verilog (Figure 1).

**Figure 1**: *Binary up down counter with bus utilization*

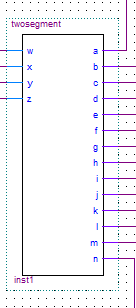


Next a seven segment display decoder is built in Verilog. This module will take the binary representation of a number and convert it to outputs of the seven segment display units for the DE1 . Two different seven segment display decoders were created one for a single display that counts in hexadecimal (Figure 2) another that outputs to two displays that count up in decimal (Figure 3).

**Figure 2:** *Single display that counts up in hexadecimal*

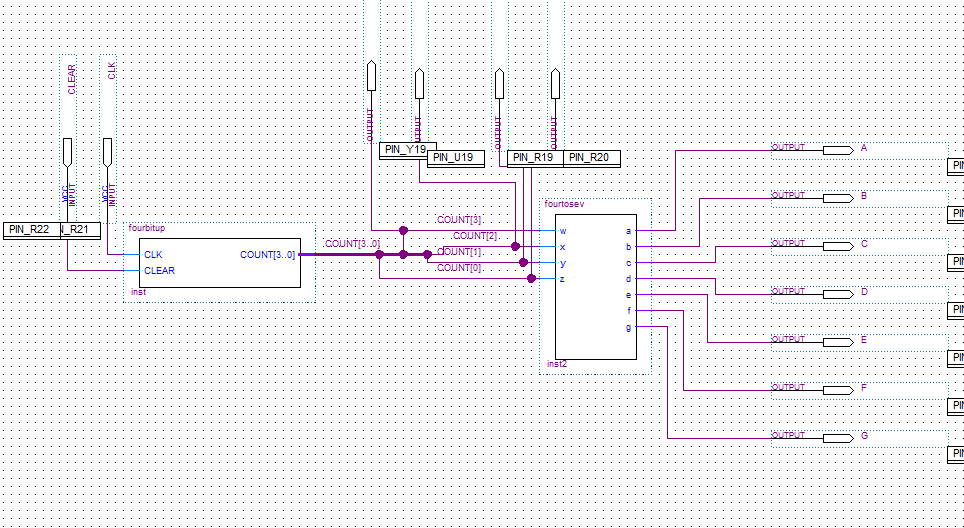
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**Figure 3:** *Double display that counts up in decimal.*

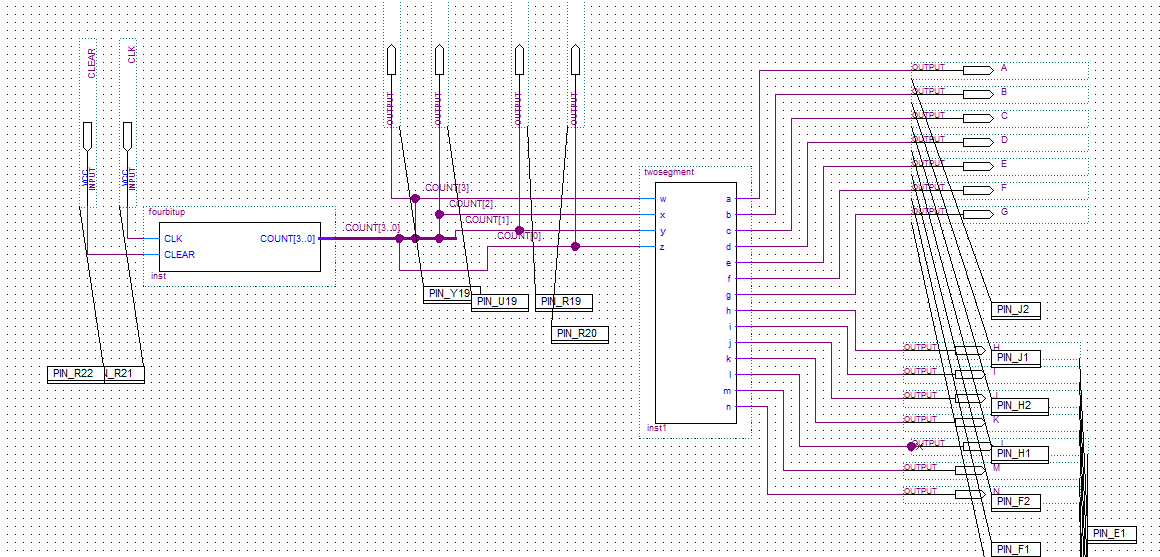


Both of these designs are then integrated into one unit and tested on the DE1 for demonstration.

**Figure 4:** *Single display integration*

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**Figure 5:** *Double display integration*

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These integrations have assigned pins to the DE1 and tested. The clock (count up) and clear are tied to the Key 1 and Key0 respectively. Once key 1 is pushed it will increase the decimal value of the display from zero to one and then again from one to two and so on until it hits ten. At this point the single display will continue to count in hexadecimal A, B, C, D. However the double display will count in decimal incrementing the second display to one and resetting the first to zero displaying a ten.

**Conclusion:** The lab was successfully demonstrated to the teaching assistant and the lab was successfully and fully completed. Since guidance was provided during the lecture session this lab went smoothly without many interruptions and a key component in leading into Verilog.